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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

BJ

Office Action Summary	Application No.	Applicant(s)
	09/822,950	THURSTON, ANDREW J.
	Examiner	**Art Unit**
	Dipakkumar Gandhi	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

pD

Response to Amendment

1. Applicant's request for reconsideration filed on 5/31/2005 has been received.

2. Applicant's arguments with respect to claims 1-55 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments, see pages 12-22 of remarks, filed 5/31/2005, with respect to claims 1-55 have been fully considered and are persuasive. The final rejection of 02/25/2005 has been withdrawn.

Claim Rejections - 35 USC § 112

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 1, "no more than six equations having no more than two branch decisions" does not clearly mention how many equations are used in the decoding and number of equations does not describe the features of the invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-6, 9-15, 17-18, 20-26, 30, 31, 32, 38, 39, 40, 42, 43, 44, 45, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US 5,583,499) in view of Wicker (Error Control Systems for Digital Communication and Storage, 1995, Prentice-Hall, Inc.).

As per claim 1, Oh et al. teach a method of decoding an error-correction code in a data signal, comprising the steps of: receiving the data signal at a decoding unit; computing a plurality of syndromes associated with the data signal using the decoding unit; and locating errors within the data signal using the error polynomial (col. 1, lines 8-13, col. 1, lines 52 to col. 2, line 1, Oh et al.).

However Oh et al. do not explicitly teach the specific use of extracting an error polynomial from the data signal based on no more than six equations having no more than two branch decisions.

Wicker in an analogous art teaches Peterson's direct-solution decoding algorithm for the coefficients of the error locator polynomial (pages 206-208, Wicker).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Oh et al.'s patent with the teachings of Wicker by including an additional step of extracting an error polynomial from the data signal based on no more than six equations having no more than two branch decisions.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that extracting an error polynomial from the data signal based on no more than six equations having no more than two branch decisions would provide the opportunity to reduce the number of circuit components and increase the decoding speed to determine the errors in the received data signal.

- As per claim 2, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the method, wherein said extracting step extracts the error polynomial in no more than 12 clock cycles (col. 2, lines 19-25, Oh et al.).

- As per claim 3, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the method, wherein said extracting step includes the step of controlling a plurality of Galois field multiply accumulators using a state machine (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

- As per claim 4, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the method, wherein each of the plurality of Galois field multiply accumulators represents a different power of the error polynomial (col. 4, lines 44-48, Oh et al.).

- As per claim 5, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein said computing, extracting, and locating steps use a Bose-chaudhuri-Hocquenghem (BCH) code (page 204, Wicker).

- As per claim 6, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the method wherein the computing steps computes 2t syndromes, where t is a number of correctable errors which the error-correcting code can correct (col. 3, lines 28-32, Oh et al.).

- As per claim 9, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method of claim 1 wherein said extracting step generates the error polynomial based on the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1 S_2$,

(3) $\sigma^1(X) = 1 + S_1 X$,

(4) if ($d_1 = 0$) then $\sigma^2(X) = \sigma^1(X)$

else if ($d_0 = 0$) then $\sigma^2(X) = q_0 \sigma^1(X) + d_1 X^3$

else $\sigma^2(X) = q_0 \sigma^1(X) + d_1 X^2$,

(5) $d_2 = S_5 \sigma 0 + S_4 \sigma 1 + S_3 \sigma 2 + S_2 \sigma 3$, and

(6) if ($d_2 = 0$) then $\sigma^3(X) = \sigma^2(X)$

else $\sigma^3(X) = q_1 \sigma^1(X) + d_1 X^3$,

where S_i are the syndromes, σ^i are minimum-degree polynomials, σ_i are four coefficients for $\sigma^2(X)$, d_0-d_2 are correction factors, q_0-q_1 are additional correction factors, q_0 is equal to d_0 unless d_0 is zero, when q_0 is 1, and q_1 is equal to d_1 unless d_1 is zero, when $q_1 = q_0$ (pages 207-208, Wicker).

- As per claim 10, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the method of claim 1 wherein said extracting step includes the step of calculating correction terms using four Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.).

- As per claim 11, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the method wherein said locating step locates the errors by determining roots of the error polynomial, which correspond to error locations (col. 1, lines 64-66, Oh et al.).

- As per claim 12, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein the locating step uses Chien's algorithm to search for the error location numbers (page 209, Wicker).

- As per claim 13, Oh et al. and Wicker teach the additional limitations.

Wicker teaches a method of determining an error polynomial for decoding a Bose-Chaudhuri-Hocquenghem (BCH) code (page 204, Wicker).

Oh et al. teach computing a plurality of syndromes associated with a data signal having a BCH code embedded therein; feeding the syndromes to a plurality of Galois field multiply accumulators; calculating a plurality of minimum-degree polynomials associated with the BCH code, using the Galois field multiply accumulators and generating an error polynomial based on the minimum-degree polynomials, said calculating and generating steps extracting the error polynomial in no more than 12 clock cycles (col. 1, line 60 to col. 2, line 34, Oh et al.).

- As per claim 14, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein said calculating step includes the step of calculating a plurality of coefficients of at least one of the minimum-degree polynomials (page 206, Wicker).

- As per claim 15, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the method wherein the calculating step includes the step of computing a first correction term using at least one of the Galois field multiply accumulators. (col. 2, lines 11-18, Oh et al.).

Wicker teaches that the first correction term being equal to a first one of the syndromes (page 208, Wicker).

- As per claim 17, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein the step of computing the first correction term includes the step of operating the at least one Galois field multiply accumulator in a pass-through mode (page 208, Wicker).

- As per claim 18, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein: the BCH code is a triple-error correcting code; and the calculating step calculates at least three minimum-degree polynomials (pages 204, 208, Wicker).

- As per claim 20, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein said calculating step includes the step of determining whether the second correction term is equal to zero (page 208, Wicker).

- As per claim 21, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein the calculating step equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the second correction term is equal to zero (page 212, Wicker).

- As per claim 22, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein the calculating step includes the step of determining whether the third correction term is equal to zero (pages 207-208, Wicker).

- As per claim 23, Oh et al. and Wicker teach the additional limitations.

Wicker teaches the method wherein the calculating step equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the third correction term is equal to zero (page 212, Wicker).

- As per claim 24, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the method wherein there are exactly four of the Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.) and the calculating step includes the step of controlling inputs to the Galois field multiply accumulators using a state machine (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

- As per claim 25, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach a circuit for generating an error polynomial of a Bose-chaudhuri-Hocquenghem (BCH) code (fig. 3, col. 1, lines 36-37, col. 3, lines 15-17, Oh et al.), comprising: a plurality of syndrome inputs; a plurality of Galois field multiply accumulators; and means for using said Galois field multiply accumulators to generate an error polynomial based on values provided at said syndrome inputs (col. 1, line 60 to col. 2, line 34, Oh et al.).

Wicker teaches generating an error polynomial executing no more than six equations with two branch decisions (page 207-208, Wicker).

- As per claim 26, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the circuit wherein said using means includes a state machine, which asserts control ports on the Galois field multiply accumulators to execute the equations (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

- As per claim 30, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the circuit wherein said using means uses the Galois field multiply accumulators to calculate a plurality of minimum-degree polynomials associated with the BCH code (fig. 3, col. 1, lines 36-37, col. 5, lines 58-63, Oh et al.).

- As per claim 31, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the circuit wherein said using means uses the Galois field multiply accumulators (fig. 3, col. 5, lines 58-63, Oh et al.).

Wicker teaches calculating a plurality of coefficients of at least one of the minimum-degree polynomials (page 206, Wicker).

- As per claim 32, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the circuit for calculating the error locator polynomial and using means uses the Galois field multiply accumulators (fig. 3, col. 5, lines 58-63, Oh et al.).

Wicker teaches that the BCH code is a triple-error correcting code; and calculating at least three minimum-degree polynomials (pages 204, 208, Wicker).

- As per claim 38, Oh et al. and Wicker teach the additional limitations.

Wicker teaches generating an error polynomial based on the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(X) = 1 + S_1X$,

(4) if $(d_1 = 0)$ then $\sigma^2(X) = \sigma^1(X)$

else if (d_0 = 0) then $\sigma^2(X) = q_0\sigma^1(X) + d_1X^3$

else $\sigma^2(X) = q_0\sigma^1(X) + d_1X^2$,

(5) $d_2 = S_5\sigma 0 + S_4\sigma 1 + S_3\sigma 2 + S_2\sigma 3$, and

(6) if (d_2 = 0) then $\sigma^3(X) = \sigma^2(X)$

else $\sigma^3(X) = q_1\sigma^1(X) + d_1X^3$,

where S_i are the syndromes, σ^i are minimum-degree polynomials, σ_i are four coefficients for $\sigma^2(X)$, d_0-d_2 are correction factors, q_0-q_1 are additional correction factors, q_0 is equal to d_0 unless d_0 is zero, when q_0 is 1, and q_1 is equal to d_1 unless d_1 is zero, when $q_1 = q_0$ (pages 207-208, Wicker).

Oh et al. teach a decoder circuit (fig. 3, col. 5, lines 58-63, Oh et al.) and a plurality of Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.); and a state machine programmed to use the Galois field multiply accumulators (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

- As per claim 39, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the decoder circuit wherein each of the Galois field multiply accumulators represents a different power of the error polynomial (table 1, table 2, table 3, col. 4, lines 9-17, lines 50-60, col. 5, lines 37-47, Oh et al.).

- As per claim 40, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the decoder circuit wherein said state machine is programmed to operate a selected one or more of said Galois field multiply accumulators (figure 1A, 1B, 1C, 3, col. 3, lines 6-12, lines 15-17, lines 22-25, col. 4, lines 3-6, col. 5, lines 58-63, col. 6, lines 3-5, Oh et al.).

Wicker teaches operating multiply accumulators in a pass-through mode (page 208, Wicker).

- As per claim 42, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the decoder circuit wherein: there are exactly four of said Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.)

Wicker teaches that the BCH code is a triple-error correcting code (pages 204, 208, Wicker).

- As per claim 43, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the decoder circuit wherein equation (1) is performed using a first one of said Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.).

- As per claim 44, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the decoder circuit wherein equation (2) is performed using said first Galois field multiply accumulator and a second one of said Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.).

- As per claim 45, Oh et al. and Wicker teach the additional limitations.

Oh et al. teach the decoder circuit wherein equation (3) is performed using said first and second Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.).

- As per claim 55, Oh et al. and Wicker teach the additional limitations.

Wicker teaches using a non-iterative algorithm to generate the error polynomial from the data signal based on no more than six equations having no more than two branch decisions (page 208, Wicker).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US 5,583,499) and Wicker (Error Control Systems for Digital Communication and Storage, 1995, Prentice-Hall, Inc.) as applied to claim 1 above, and further in view of Erhart et al. (US 5,051,999).

As per claim 7, Oh et al. and Wicker substantially teach the claimed invention described in claim 1 (as rejected above).

However Oh et al. and Wicker do not explicitly teach the specific use of the method wherein the computing step uses a linear feedback register to compute the syndromes.

Erhart et al. in an analogous art teach that each shift of the linear feedback register calculates a subsequent syndrome (col. 3, lines 40-41, Erhart et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Oh et al.'s patent with the teachings of Erhart et al. by including an additional step of using the method wherein the computing step uses a linear feedback register to compute the syndromes. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method wherein the computing step uses a linear feedback register to compute the syndromes would provide the opportunity to use a programmable linear feedback register programmed with a feedback value corresponding to the

generator polynomial and the programmable linear feedback register can be further programmed to receive the n bits of data and calculate syndromes.

9. Claims 8, 16, 19, 27-29, 33, 34, 35, 36, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US 5,583,499) and Wicker (Error Control Systems for Digital Communication and Storage, 1995, Prentice-Hall, Inc.) as applied to claim 1, 13 above, and further in view of Stenerson (US 4,597,083).

As per claim 8, Oh et al. and Wicker substantially teach the claimed invention described in claim 1 (as rejected above).

However Oh et al. and Wicker do not explicitly teach the specific use of the method wherein the computing step includes the steps of: dividing a received code word in the data signal by a minimal Galois polynomial; and evaluating a remainder from said dividing step.

Stenerson in an analogous art teaches that codeword is divisible by a code generator polynomial in the form of a product of a plurality of different factors in the form (x+a.sup.i). Four syndrome signals are derived, each corresponding to a respective first order syndrome equal to the remainder upon dividing a received data block word by a respective factor (abstract, Stenerson).

Stenerson also teaches that the received codeword may be passed through a re-encoder (also known as a syndrome generator), which produces as its output the remainder of the polynomial division s(x)=Remainder [R(x)/g(x)], (col. 4, lines 47-59, Stenerson).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Oh et al.'s patent with the teachings of Stenerson by including an additional step of using the method wherein the computing step includes the steps of: dividing a received code word in the data signal by a minimal Galois polynomial; and evaluating a remainder from said dividing step.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method wherein the computing step includes the steps of: dividing a received code word in the data signal by a minimal Galois polynomial; and evaluating a remainder from said dividing step would provide the opportunity to

determine error syndromes that can be used with further calculation to determine location of the errors and error values in the code word received.

- As per claim 16, Oh et al., Wicker and Stenerson teach the additional limitations.

Stenerson teach the method wherein said calculating step includes the step of computing a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes (col. 7, line 60-64, col. 18, lines 28-33, Stenerson).

- As per claim 19, Oh et al., Wicker and Stenerson teach the additional limitations.

Oh et al. teach the Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.).

Wicker teaches computing a first correction term, the first correction term being equal to a first one of the syndromes (page 208, Wicker) and computing the third correction term being based in part on coefficients of at least one of the minimum-degree polynomials (page 208, Wicker).

Stenerson teaches computing a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes (col. 7, line 62-63, col. 18, lines 28-33, Stenerson).

- As per claim 27, Oh et al., Wicker and Stenerson teach the additional limitations.

Stenerson teaches the circuit wherein the using means computes a first correction term using at least one of the Galois field multiply accumulators, by assigning a value of a first one of the syndromes to the first correction term (col. 9, lines 44-46, col. 18, lines 28-33, Stenerson).

- As per claim 28, Oh et al., Wicker and Stenerson teach the additional limitations.

Stenerson teaches the circuit wherein the using means further computes a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes (col. 7, line 62-63, col. 18, lines 28-33, Stenerson).

- As per claim 29, Oh et al., Wicker and Stenerson teach the additional limitations.

Stenerson teaches the circuit wherein said using means computes the first correction term by operating at least one Galois field multiply accumulator in a pass-through mode (col. 18, lines 28-33, col. 22, lines 30-34, Stenerson).

- As per claim 33, Oh et al., Wicker and Stenerson teach the additional limitations.

Oh et al. teach teaches the circuit wherein the using means uses the Galois field multiply accumulators (col. 4, lines 3-6, Oh et al.).

Wicker teaches computing a first correction term, by assigning a value of a first one of the syndromes to the first correction term (page 208, Wicker) and computing a third correction term, the third correction term being based in part on coefficients of at least one of the minimum-degree polynomials (page 208, Wicker).

Stenerson teaches computing a second correction term, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes (col. 7, line 62-63, col. 18, lines 28-33, Stenerson).

- As per claim 34, Oh et al., Wicker and Stenerson teach the additional limitations.

Oh et al. teach the circuit for calculating the error locator polynomial (fig. 3, col. 5, lines 58-63, Oh et al.).

Wicker teaches determining whether the second correction term is equal to zero (page 208, Wicker).

- As per claim 35, Oh et al., Wicker and Stenerson teach the additional limitations.

Oh et al. teach the circuit for calculating the error locator polynomial (fig. 3, col. 5, lines 58-63, Oh et al.).

Wicker teaches equating a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the second correction term is equal to zero (page 212, Wicker).

- As per claim 36, Oh et al., Wicker and Stenerson teach the additional limitations.

Oh et al. teach the circuit for calculating the error locator polynomial (fig. 3, col. 5, lines 58-63, Oh et al.).

Wicker teaches determining whether the third correction term is equal to zero (pages 207-208, Wicker).

- As per claim 37, Oh et al., Wicker and Stenerson teach the additional limitations.

Oh et al. teach the circuit for calculating the error locator polynomial (fig. 3, col. 5, lines 58-63, Oh et al.).

Wicker teaches equating a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the third correction term is equal to zero (page 212, Wicker).

10. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US 5,583,499) and Wicker (Error Control Systems for Digital Communication and Storage, 1995, Prentice-Hall, Inc.) as applied to claim 38 above, and further in view of Wolf (US 6,385,751 B1).

As per claim 41, Oh et al. and Wicker substantially teach the claimed invention described in claim 38 (as rejected above).

However Oh et al. and Wicker do not explicitly teach the specific use of the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit.

Wolf in an analogous art teaches that Reed-Solomon encoders/decoders have been built using chip sets consisting of ASIC (Application Specific Integrated Circuit) processor elements (col. 3, lines 47-49, Wolf). Wolf also teaches that each of the blocks Reed-Solomon control block 403, Galois Field encoder setup block 422, Galois Field decoder setup block 423, encoder 457 and the decoder 458 illustrated in FIG. 4 include a state machine. The state machine flow is illustrated in FIG. 8 (figure 4, 8, col. 10, lines 50-54, Wolf).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Oh et al.'s patent with the teachings of Wolf by including an additional step of using the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoder circuit wherein the state machine and the Galois field multiply accumulators are formed in a common application-specific integrated circuit would provide the opportunity to reduce the number of circuit elements and increase the processing speed of Galois field multiply accumulators and the decoder circuit for error correction.

11. Claims 46-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. (US 5,583,499) and Wicker (Error Control Systems for Digital Communication and Storage, 1995, Prentice-Hall, Inc.) as applied to claim 38 above, and further in view of Maki et al. (US 4,873,688).

As per claim 46, Oh et al. and Wicker substantially teach the claimed invention described in claim 38 (as rejected above).

However Oh et al. and Wicker do not explicitly teach the specific use of the decoder circuit wherein: at least one of said Galois field multiply accumulators has a first multiplexer whose output is coupled to a first input of a Galois field multiplier, a second multiplexer whose output is coupled to a second input of said Galois field multiplier, and a third multiplexer whose output is coupled to a first input of a Galois field adder, wherein an output of said Galois field multiplier is further coupled to a second input of said Galois field adder; and said state machine controls respective select lines for each of said multiplexers.

Maki et al. in an analogous art teach

"8. A Galois Field Euclid Algorithm apparatus for operating on an arbitrary received polynomial R(x), for calculating a magnitude polynomial, .OMEGA..sub.i (x) having a first plurality of coefficients and a location polynomial, .LAMBDA..sub.i (x), having a second plurality of coefficients, said magnitude polynomial representing a magnitude of an error in said received polynomial and said location polynomial representing a location of said error in said received polynomial for use with a code having t correctable errors, said apparatus comprising:

a. a Euclid Algorithm divide module coupled to receive said received polynomial for implementing a first equation set forth below: .OMEGA..sub.i

(x)=.OMEGA..sub.i-2 (x) mod .OMEGA..sub.i-1 (x); and

b. a Euclid Algorithm multiply module coupled to receive said received

polynomial for implementing a second equation set forth below: .LAMBDA..sub.i

(x)=-q.sub.i (x).LAMBDA..sub.i-1 (x)+.LAMBDA..sub.i-2 (x).

9. The Galois Field Euclid Algorithm apparatus according to claim 8 (Maki et al.) wherein:

a. said divide module comprises:

(1) a quotient bus;

(2) a plurality of first cells, each first cell having:

(a) a first input and a first output;

(b) a first register having a second input and a second output, said second input coupled to a said first input;

(c) a second register having a third input and a third output;

(d) a first 2 input/2 output multiplexer coupled to receive having a fourth input, a fifth input, a fourth output and a fifth output, said fourth input coupled to said second output, said fifth input coupled to said third output and said fourth output coupled said third input; and

(e) a first Galois Field multiplier having a sixth input, a seventh input and a sixth output, said sixth input coupled to said fourth output and to said third input and said seventh input coupled to said quotient bus;

(f) a Galois Field adder having an eighth input, a ninth input and a seventh output, said eighth input coupled to said sixth output, said ninth input coupled to said fifth output and said seventh output coupled to said first output; and

(3) a second cell having:

(a) a third register having a tenth input and an eighth output;

(b) a fourth register having an eleventh input and a ninth output;

(c) a second 2 input/2 output multiplexer having a twelfth input, a thirteenth input, a tenth output and an eleventh output said eighth output coupled to said twelfth input, said ninth output coupled to said thirteenth input and said eleventh output coupled to said eleventh input;

(d) means for calculating an inverse value having a twenty-second input and an eighteenth output, said twenty-second input coupled to said eighth output;

(e) a latch means having a twenty-third input and a nineteenth output, said twenty-third input coupled to said eighteenth output; and

(f) a second Galois Field multiplier having a twenty-fourth input, a twenty-fifth input and a twentieth output, said twenty-fourth input coupled to said nineteenth output, said twenty-fifth input coupled to said tenth output and said twentieth output coupled to said quotient bus; and

b. said multiply module comprises:

(1) said quotient bus; and

(2) a plurality of third cells, each said third cell having:

(a) a first register having a fourteenth input and a twelfth output;

(b) a second register having a fifteenth input and a thirteenth output;

(c) a third 2 input/2 output multiplexer having a sixteenth input, a seventeenth input, a fourteenth output and a fifteenth output, said sixteenth
input coupled to said twelfth output;

(d) a Galois Field multiplier having an eighteenth input, a nineteenth input
and a sixteenth output, said eighteenth input coupled to said fifteenth output
and said nineteenth input coupled to said quotient bus; and

(e) a Galois Field adder having a twentieth input, a twenty-first input and a seventeenth output, said twentieth input coupled to said sixteenth output, said twenty-first input coupled to said fourteenth output and said seventeenth output coupled to said fourteenth input" (figure 9a, 9b, 9c, col. 19, line 12 – col. 20, line37, Maki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Oh et al.'s patent with the teachings of Maki et al. by including an additional step of using the decoder circuit wherein: at least one of said Galois field multiply accumulators has a first multiplexer whose output is coupled to a first input of a Galois field multiplier, a second multiplexer whose output is coupled to a second input of said Galois field multiplier, and a third multiplexer whose output is coupled to a first input of a Galois field adder, wherein an output of said Galois field multiplier is further coupled to a second input of said Galois field adder; and said state machine controls respective select lines for each of said multiplexers.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to use the Galois field multiply accumulators and multiplexers to generate an error polynomial that can be used to determine the location of errors in the code word.

- As per claim 47, Oh et al., Wicker and Maki et al. teach the additional limitations.

Maki et al. teach the decoder circuit further comprising means for determining when an output of said Galois field adder is equal to zero (col. 9, lines 22-30, Maki et al.).

12. Claims 48, 49, 50, 51, 52, 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1) in view of Kraft (US 5,343,481).

As per claim 48, Alvarez et al. teach an 0C-192 input/output card comprising: four OC-48 processors; and an OC-192 front-end application-specific integrated circuit (ASIC) connected to said four OC-48 processors, said OC-192 front-end ASIC having means for de-interleaving an OC-192 signal to create four OC-48 signals (figure 17, page 12, paragraphs 192-193, page 30, paragraph 470, Alvarez et al.).

However Alvarez et al. do not explicitly teach the specific use of means for decoding error-correction codes embedded in each of the four OC-48 signals, said decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles and the decoding means uses a non-iterative algorithm to generate the error polynomial.

However Kraft in an analogous art teaches that the current invention teaches the non-iterative use of a decision tree with closed formulas over the Galois Field for the polynomial coefficients (col. 4, lines 35-38, Kraft). Kraft also teaches that this invention teaches a combinational circuit with no clocks and no sequential operations (col. 4, lines 39-41, Kraft). Kraft teaches that the object of the present invention...Galois Field GF (col. 4, lines 50-57, Kraft).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Kraft by including an additional step of using means for decoding error-correction codes embedded in each of the four OC-48 signals, said decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles and the decoding means uses a non-iterative algorithm to generate the error polynomial.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to find the error-location polynomial in a short time with several very fast computations over the Galois Field.

- As per claim 49, Alvarez et al. and Kraft teach the additional limitations.

Kraft teaches that the decoding means includes a plurality of Galois field multiply accumulators (fig. 3, col. 8, lines 12-22, Kraft).

- As per claim 50, Alvarez et al. and Kraft teach the additional limitations.

Kraft teaches that decoding means further includes a state machine (fig. 2, 4, col. 8, lines 61-64, Kraft) for controlling the Galois field multiply accumulators (fig. 3, col. 8, lines 12-22, Kraft).

- As per claim 51, Alvarez et al. and Kraft teach the additional limitations.

Kraft teaches that the decoding means uses the Galois field multiply accumulators to generate an error polynomial for a Bose-chaudhuri-Hbcquenghem (BCH) triple-error correcting code (col. 4, lines 23-27, Kraft).

- As per claim 52, Alvarez et al. and Kraft teach the additional limitations.

Kraft teaches that the decoding means includes no more than four of said Galois field multiply accumulators (fig. 3, col. 8, lines 12-22, Kraft).

- As per claim 53, Alvarez et al. and Kraft teach the additional limitations.

Kraft teaches that decoding means includes means for computing a plurality of BCH syndromes which are used by said Galois field multiply accumulators to generate the error polynomial (fig. 1, 2, 3, col. 7, line 8 to col. 8, line 60, col. 10, lines 51-65, Kraft).

13. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alvarez et al. (US 2002/0165962 A1) and Kraft (US 5,343,481) as applied to claim 48 above, and further in view of Wicker (Error Control Systems for Digital Communication and Storage, 1995, Prentice-Hall, Inc.).

As per claim 54, Alvarez et al. and Kraft substantially teach the claimed invention described in claim 48 (as rejected above).

However Alvarez et al. and Kraft do not explicitly teach the specific use of the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers.

Wicker in an analogous art teaches that once the error locator polynomial is known, the roots can be located through the use of the Chien search. The Chien search is a systematic means of evaluating the error locator polynomial at all elements in a GF field (fig. 9-1, pages 208-209, Wicker).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Alvarez et al.'s patent with the teachings of Wicker by including an additional step of using the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the decoding means that locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers would provide the opportunity to determine the location of all the errors in the code word by determining all roots of the error locator polynomial.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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